# JMM4708ND

## *Product Preview*

## 30V N-Channel MOSFET

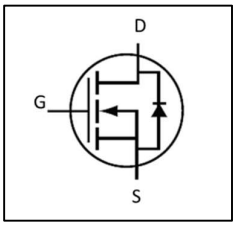
## Features

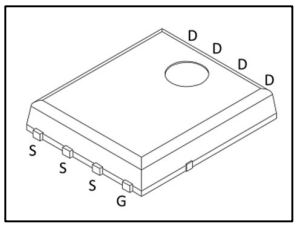
- Advanced shielded-gate technology
- Ultra-low on-resistance and gate-charge
- RoHS compliant
- 100% avalanche tested

| Product Summary | |
|---|---|
| $V_{DS}$ | 30V |
| $R_{DS(ON)}$ | 2.0 mΩ (Typ.) |
| | 2.5 mΩ (Max.) |

## Applications

- Motor controllers
- DC-to-DC convertors
- Battery-driven electronic products, electrical equipment and machines




## Ordering Information

| Part Number | Marking | Package | Packaging |
|---|---|---|---|
| JMM4708ND | MM4708ND | DFN5x6 | Tape & Reel |

## Absolute Maximum Ratings

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Drain-to-Source Voltage | $V_{DS}$ | 30 | V |
| Gate-to-Source Voltage | $V_{GS}$ | ±20 | |
| Continuous Drain Current, Silicon limited ($T_C$ = 25°C) (1) | $I_D$ | 120 | A |
| Continuous Drain Current, Silicon limited ($T_C$ = 100°C) (1) | $I_D$ | 75 | |
| Continuous Drain Current, Silicon limited ($T_A$ = 25°C) (2), (5) | $I_D$ | 24 | |
| Continuous Drain Current, Silicon limited ($T_A$ = 100°C) (2), (5) | $I_D$ | 15 | |
| Pulsed Drain Current (3) | $I_{DM}$ | 480 | |
| Power Dissipation ($T_C$ = 25°C) | $P_D$ | 56.8 | W |
| Linear Derating Factor | - | 0.45 | W/°C |
| Single Pulse Avalanche Energy (4) | $E_{AS}$ | 83.5 | mJ |
| Avalanche Current (4) | $I_{AS}$ | 26 | A |
| Junction Temperature | $T_J$ | -55 to 150 | °C |
| Storage Temperature | $T_{STG}$ | -55 to 150 | |

## Thermal Characteristics

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Junction-to-Ambient Thermal Resistance (5) | $R_{\theta JA}$ | 55 | °C/W |
| Junction-to-Case Thermal Resistance | $R_{\theta JC}$ | 2.2 | |

## Static Electrical Characteristics (6)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Drain-to-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250μA | 30 | - | - | V |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 1.1 | - | 2.2 | |
| Drain-to-Source Leakage Current | $I_{DSS}$ | $V_{DS}$ = 30V, $V_{GS}$ = 0V | - | - | 1 | μA |
| Gate-to-Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0V, $V_{GS}$ = ±20V | - | - | ±100 | nA |
| Drain-to-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$ = 10V, $I_D$ = 20A | - | 2.0 | 2.5 | mΩ |
| | | $V_{GS}$ = 4.5V, $I_D$ = 20A | - | 3.0 | 3.8 | mΩ |

## Dynamic Electrical Characteristics (6)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 5V, $I_D$ = 20A | - | 90 | - | S |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10V, | - | 29.5 | - | nC |
| Gate-to-Source Charge | $Q_{gs}$ | $V_{DS}$ = 15V, | - | 6.0 | - | |
| Gate-to-Drain Charge | $Q_{gd}$ | $I_D$ = 20A | - | 5.5 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{GS}$ = 10V, | - | 15 | - | ns |
| Rise Time | $t_r$ | $V_{DS}$ = 15V, | - | 5 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | $I_D$ = 20A, | - | 35 | - | |
| Fall Time | $t_f$ | $R_G$ = 3.0Ω | - | 9 | - | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0V, | - | 2225 | - | pF |
| Output Capacitance | $C_{oss}$ | f = 1MHz, | - | 986 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | $V_{DS}$ = 15V | - | 100 | - | |

## Diode Characteristics (6)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_{SD}$ | $V_{GS}$ = 0V, $I_S$ = 10A | - | 0.8 | - | V |
| Reverse Recovery Time | $t_{rr}$ | $V_{GS}$ = 0V, $I_S$ = 10A, | - | 24 | - | ns |
| Reverse Recovery Charge | $Q_{rr}$ | $dI_S/dt$ = 100A/μs | - | 30 | - | nC |

(1) Rated according to $R_{\theta JC}$.

(2) Rated according to $R_{\theta JA}$.

(3) Limited by maximum $T_J$.

(4) $T_A$ = 25°C, L = 0.1mH, $I_{AS}$ = 26A.

(5) Surface−mounted on 1 inch² FR4 board, 2 oz Cu.

(6) $T_J$ = 25°C unless otherwise specified.

## Typical Electrical Characteristics

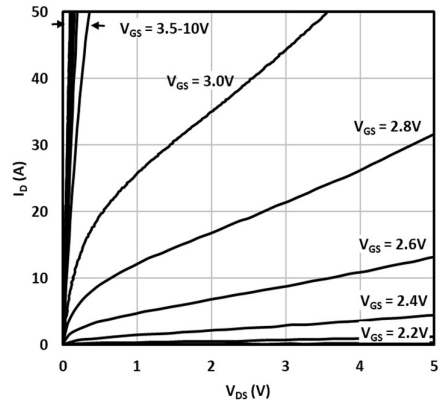



Fig. 1 Output characteristics

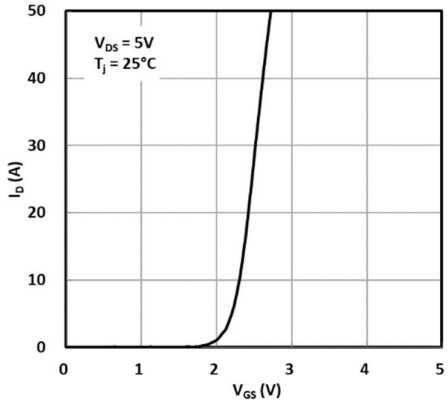



Fig. 2 Transfer characteristics

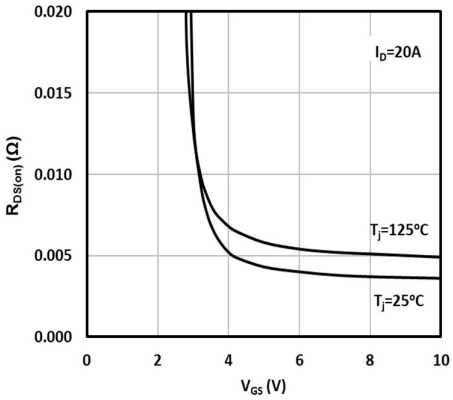



Fig.3 On-resistance vs. gate voltage

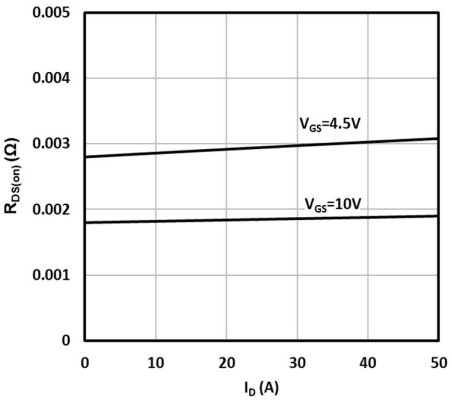



Fig.4 On-resistance vs. drain current

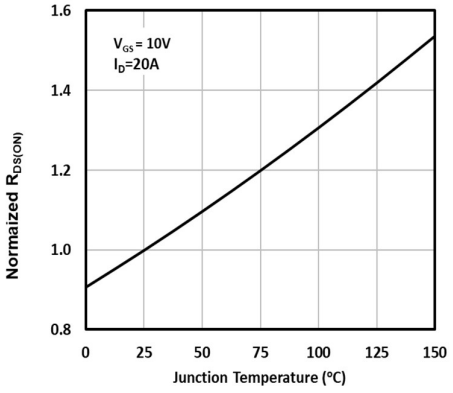



Fig.5 Normalize on-resistance vs. temperature

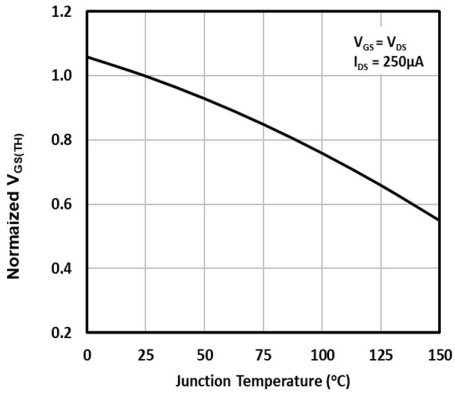



Fig.6 Normalized gate threshold voltage vs. temperature

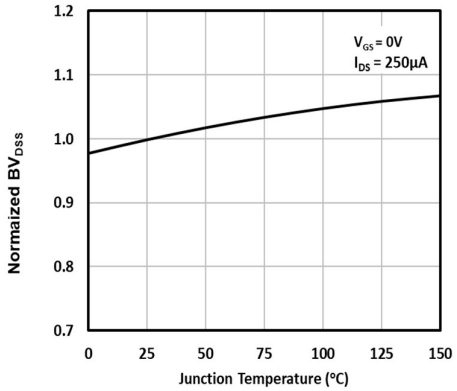



Fig.7 Normalize drain-to-source breakdown voltage vs. temperature

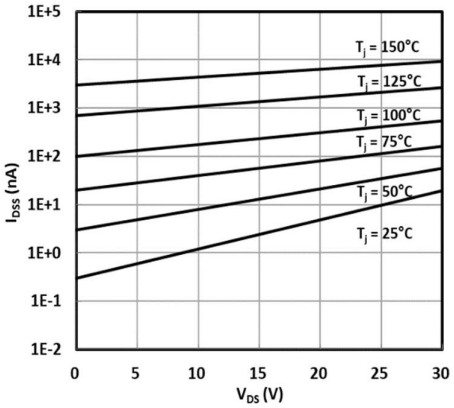



Fig.8 rain-to-source leakage current vs. voltage

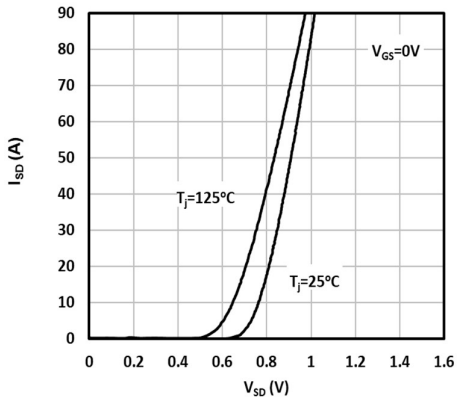



Fig.9 Source-to-drain diode forward characteristics

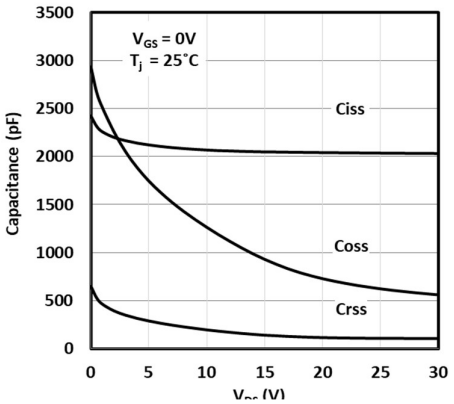



Fig.10 Capacitance vs. drain-to-source voltage

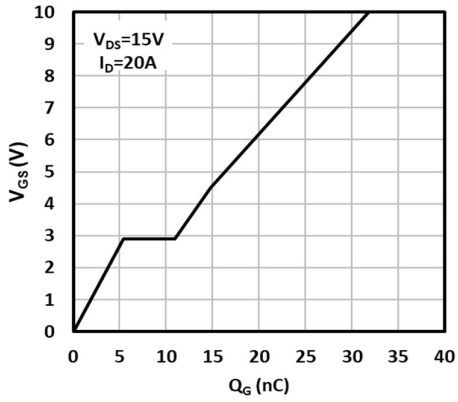



Fig.11 Gate-to-source voltage vs. gate charge

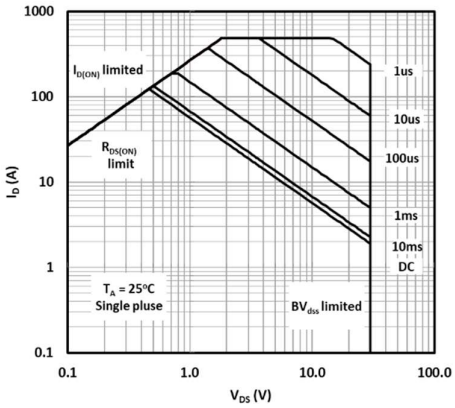



Fig.12 Safe operating area

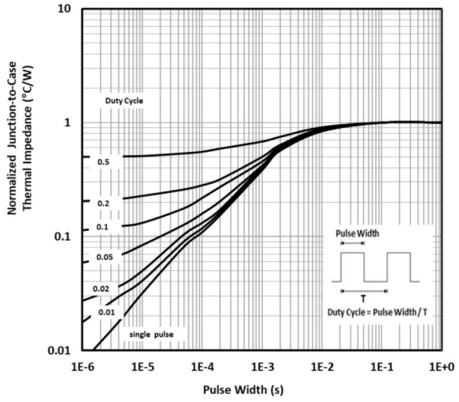



**Fig.13 Junction-to-case thermal impedance**

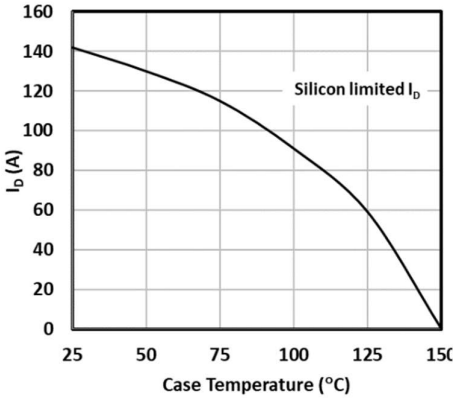



**Fig.14 Maximum drain current vs. case temperature**

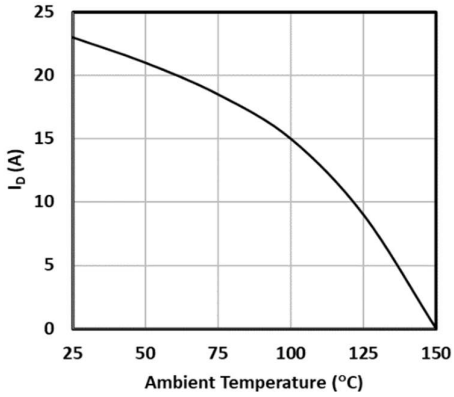
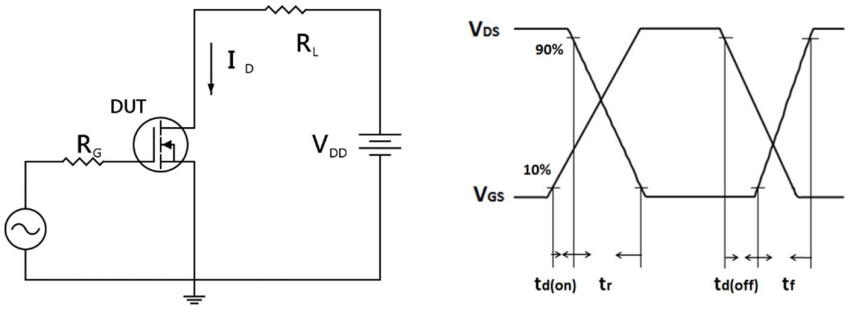
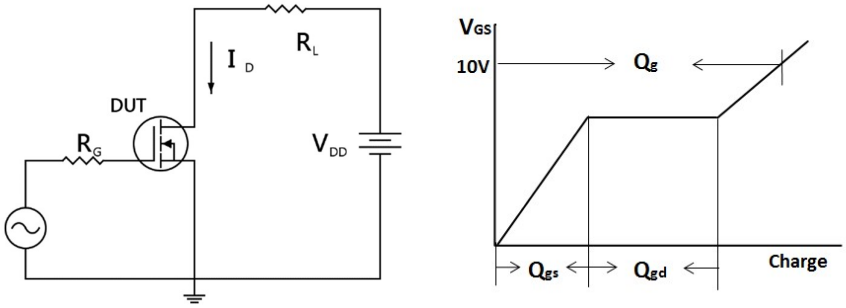



**Fig. 15 Maximum drain current vs. ambient temperature**

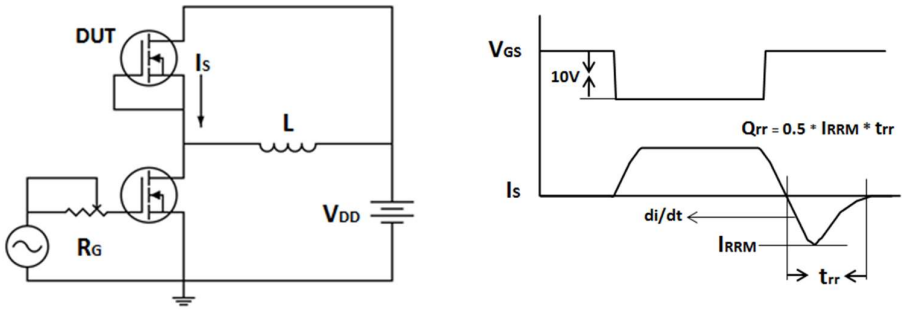
## Test Circuits and Waveforms



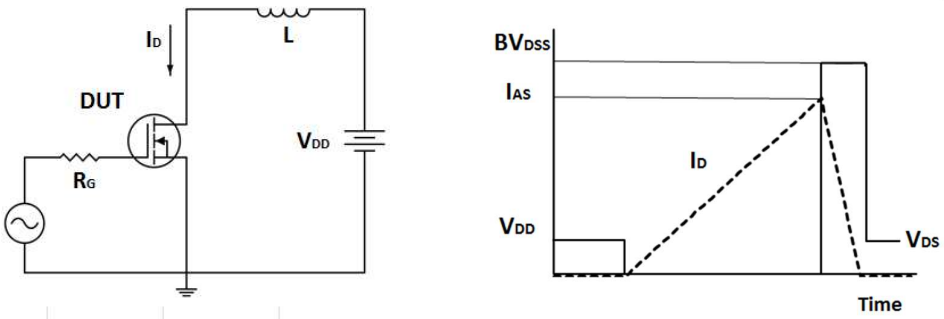

**Resistive switching time test circuit & waveforms**




**Gate charge test circuit & waveform**

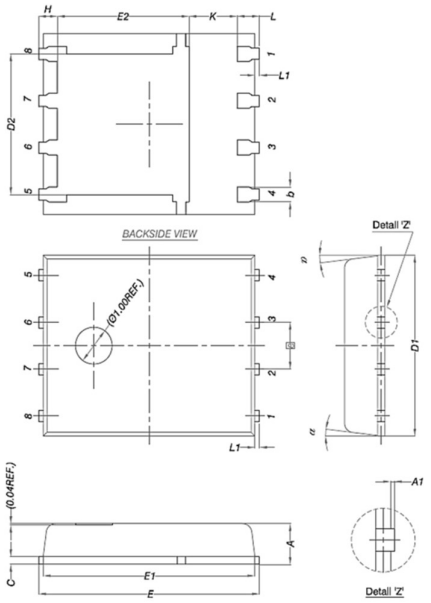



**Peak diode recovery dv/dt test circuit & waveforms**




**Unclamped inductive switching test circuit & waveforms**

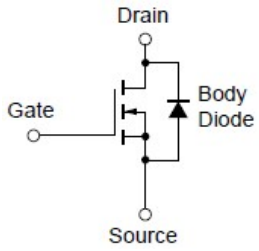
## Package Drawing




| DIM. | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0 | - | 0.05 |
| b | 0.33 | 0.41 | 0.51 |
| C | 0.20 | 0.25 | 0.30 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.61 | 3.81 | 3.96 |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 5.70 | 5.75 | 5.80 |
| E2 | 3.38 | 3.58 | 3.78 |
| e | 1.27 BSC | | |
| H | 0.41 | 0.51 | 0.61 |
| K | 1.10 | - | - |
| L | 0.51 | 0.61 | 0.71 |
| L1 | 0.06 | 0.13 | 0.20 |
| α | 0° | - | 12° |

**DFN 5x6**

## Equivalent Circuit



**Revision history of JMM4708ND specification**

| Version | Change Items | Effective Date |
|---|---|---|
| 1.00 | Initial Release | 22-May-20 |
| 1.01 | Remove Continuous Drain Current, Package Limited. | 27-Aug-20 |
| 1.02 | Updated Pulsed Drain Current $I_{DM}$.<br>Updated characteristic curve under different temperature.<br>Updated Gate charge test circuit. | 04-Dec-20 |

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